



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:  
James B. Johnson et al.

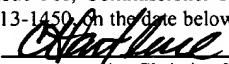
Serial No.: 09/809,608

Filed: March 15, 2001

For: Method and Apparatus for  
Compensating Duty Cycle Distortion in  
a Data Output Signal From a Memory  
Device by Delaying and Distorting a  
Reference Clock

§ Group Art Unit: 2116  
§  
§ Examiner: Trujillo, James K.  
§  
§ Atty. Docket: MICS: 0070/FLE  
§ (00-0917)  
§

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below:	
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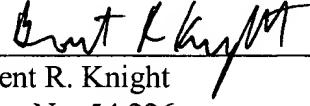
Sir:

**TRANSMITTAL OF FORMAL DRAWINGS**

Enclosed are six (6) sheets of formal drawings for the above-referenced patent application, which are attached as Appendix A.

Respectfully submitted,

Date: November 19, 2004

  
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